Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

a first terminal configured for connection to a positive plate of the first capacitor;

a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

a third terminal configured for connection to a negative plate of the second capacitor; and

an active element integrated within the inductor-free circuitry between the first, second, and third terminals and adapted to substantially balance the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is an op amp, the op amp having an input, an output, and a feedback loop, the input being connected to two voltage dividing resistors, the output being connected to the second terminal through a current limiting resistor, wherein an end of the feedback loop is connected between the output and the current limiting resistor.

2. (canceled)

3. (canceled)

4. (canceled)

5. (currently amended): The module of claim ~~2~~1, wherein the feedback loop includes a feedback resistor.

6. (currently amended): A ~~The~~ module ~~of claim 1~~ having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

a first terminal configured for connection to a positive plate of the first capacitor;

a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

a third terminal configured for connection to a negative plate of the second capacitor; and

an active element integrated within the inductor-free circuitry between the first, second, and third terminals and adapted to substantially balance the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is a switched voltage converter that incorporates a flying capacitor.

7. (canceled)

8. (original): The module of claim 1, wherein at least one of the terminals is further configured for connection to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.

9. (original): The module of claim 8, wherein the first and second modules' inductor-free circuitries are substantially identical.

10. (original): The module of claim 8 wherein the first and second modules' circuitry overlap upon connection to the second module.

11. (original): The module of claim 10, wherein the first and second module's circuitry overlap at one of the terminals.

12. (original): The module of claim 10, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.

13-19. (canceled)

20 (currently amended): A method for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

forming a first terminal configured for connection to a positive plate of the first capacitor;

forming a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

forming a third terminal configured for connection to a negative plate of the second capacitor; and

integrating an active element within an inductor-free circuitry between the first, second, and third terminals such that the active element substantially balances the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is an op amp, the op amp having an input, an output, and a feedback loop, wherein integrating the active element comprises:

connecting the input to two voltage dividing resistors;

connecting the output to the second terminal through a current limiting resistor; and

connecting an end of the feedback loop between the output and the current limiting resistor.

21. (canceled)

22. (canceled)

23. (canceled)

24. (currently amended): The method of claim 20~~1~~, wherein the feedback loop includes a feedback resistor.

25. (currently amended): A ~~The~~ method ~~of claim 20~~ for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

forming a first terminal configured for connection to a positive plate of the first capacitor;

forming a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

forming a third terminal configured for connection to a negative plate of the second capacitor; and

integrating an active element within an inductor-free circuitry between the first, second, and third terminals such that the active element substantially balances the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third

terminals, wherein the active element is a switched voltage converter that incorporates a flying capacitor.

26. (canceled)

27. (previously presented): The method of claim 20, comprising:

connecting at least one of the terminals to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.

28. (previously presented): The method of claim 27, wherein the first and second modules are substantially identical.

29. (previously presented): The method of claim 27, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules upon connection to the second module.

30. (previously presented): The method of claim 29, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules at one of the terminals.

31. (previously presented): The method of claim 29, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules across a common capacitor shared by the two pairs of capacitors.

32 (previously presented): The module of claim 1, wherein the power connections are 1) between a V+ terminal of the active element and the first terminal; and 2) between a V- terminal of the active element and the third terminal.

33. (new): The module of claim 8, wherein the first and second modules' inductor-free circuitries are identical.

34. (new): The module of claim 33 wherein the first and second modules' circuitry overlap upon connection to the second module.

35. (new): The module of claim 34, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.